WHAT IS CLAIMED IS:

1. A memory module comprising:

a generally planar printed circuit board comprising an edge, a common signal trace connector area along the edge, and a first side, the printed circuit board having a first lateral portion and a second lateral portion;

a first row of memory integrated circuits identical to one another, the first row positioned on the first side of the printed circuit board, the first row being in proximity to the common signal trace connector area, the integrated circuits of the first row having a first orientation direction, the first row having a first number of integrated circuits on the first lateral portion and a second number of integrated circuits on the second lateral portion;

a second row of memory integrated circuits identical to the integrated circuits of the first row, the second row positioned on the first side of the printed circuit board, the second row being located physically farther from the common signal trace connector than is the first row, the integrated circuits of the second row having a second orientation direction at a non-zero angle relative to the first orientation direction, the second row having a third number of integrated circuits on the first lateral portion and a fourth number of integrated circuits on the second lateral portion;

a first addressing register comprising at least one register integrated circuit, the first addressing register coupled to the integrated circuits of the first row on the first lateral portion and coupled to the integrated circuits of the second row on the first lateral portion; and

a second addressing register comprising at least one register integrated circuit, the second addressing register coupled to the integrated circuits of the first row on the second lateral portion and coupled to the integrated circuits of the second row on the second lateral portion.

2. The memory module of Claim 1, wherein the first row is substantially parallel to the edge.

3. The memory module of Claim 1, wherein the second row is substantially parallel to the edge.

4. The memory module of Claim 1, wherein the memory integrated circuits comprise Double Data Rate SDRAM integrated circuits.

5. The memory module of Claim 1, wherein the non-zero angle is approximately 180 degrees.

6. The memory module of Claim 1, wherein:

the printed circuit board has a line of bilateral symmetry which is substantially perpendicular to the edge;

the line of bilateral symmetry bisects the first side into a first lateral half and a second lateral half;

the first lateral portion comprises the first lateral half; and

the second lateral portion comprises the second lateral half.

7. The memory module of Claim 6, wherein the first number equals the second number.

8. The memory module of Claim 6, wherein the third number equals the fourth number.

9. The memory module of Claim 6, wherein the first number equals the second number, the third number equals the fourth number, and the first number is less than the third number.

10. The memory module of Claim 9, wherein the first number is at least four.

11. The memory module of Claim 9, wherein the third number is at least five.

12. The memory module of Claim 1, wherein the memory module further comprises:

a first plurality of data lines electrically connecting data pins of the first row of integrated circuits to the common signal trace connector area; and

a second plurality of data lines electrically connecting data pins of the second row of integrated circuits to the common signal trace connector area, whereby lengths of corresponding data lines of the first plurality of data lines and the second plurality of data lines are substantially the same.

13. The memory module of Claim 1, wherein the first addressing register and the second addressing register access data bits of non-contiguous subsets of a data word.

14. The memory module of Claim 13, wherein:

the first addressing register accesses data bits 0 to 15 and data bits 32 to 47; and

the second addressing register accesses data bits 16 to 31 and data bits 48 to 63.

15. The memory module of Claim 1, wherein the memory module has a height of approximately two inches and a width of approximately 5¼ inches.

16. The memory module of Claim 1, further comprising:

a third row of memory integrated circuits identical to the integrated circuits of the first row, the third row positioned on a second side of the printed circuit board, the third row being in proximity to the common signal trace connector area, the integrated circuits of the third row having a third orientation direction, the first row and the third row having the same number of integrated circuits on the first lateral portion and the first row and the third row having the same number of integrated circuits on the second lateral portion; and

a fourth row of memory integrated circuits identical to the integrated circuits of the first row, the fourth row positioned on the second side of the printed circuit board, the fourth row being located physically farther from the common signal trace connector than is the third row, the integrated circuits of the fourth row having a fourth orientation direction at a non-zero angle relative to the third orientation direction, the second row and the fourth row having the same number of integrated circuits on the first lateral portion and the second row and the fourth row having the same number of integrated circuits on the second lateral portion,

wherein the first addressing register is coupled to the integrated circuits of the third row on the first lateral half and to the integrated circuits of the fourth row on the first lateral half and the second addressing register is coupled to the integrated circuits of the third row on the second lateral half and to the integrated circuits of the fourth row on the second lateral half.

17. The memory module of Claim 16, wherein the third orientation direction is substantially the same as the first orientation direction, and the fourth orientation direction is substantially the same as the second orientation direction.